Electronic Version
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Claims

[c1] 1.A cross-coupled inverter comprising:
a first inverter circuit including a first NFET coupled to a first PFET, the first NFET and the first PFET each having a body and a drain; and
a second inverter circuit cross-coupled with the first inverter circuit at a plurality of nodes, the second inverter circuit including a second NFET coupled to a second PFET, the second NFET and the second PFET each having a body and a drain;
wherein the body of at least one of the first NFET, the second NFET, the first PFET and the second PFET is coupled so as to form a feedback path that reduces discharging at one or more of the plurality of nodes in response to a soft error event at the cross-coupled inverter.

[c2] 2.The cross-coupled inverter of claim 1 wherein:
the body and the drain of the first NFET are coupled together;
the body and the drain of the first PFET are coupled together;
the body and the drain of the second NFET are coupled

together; and
the body and the drain of the second PFET are coupled together.

[c3] 3.The cross-coupled inverter of claim 2 wherein the body and the
drain of the first NFET are coupled to the body and the drain of the first PFET.

[c4] 4.The cross-coupled inverter of claim 2 wherein the body and the drain of the second NFET are coupled to the body and the drain of the second PFET.

[c5] 5.The cross-coupled inverter of claim 2 wherein the first NFET, the second NFET, the first PFET and the second PFET each comprises a silicon-on-insulator metal-ox-ide-semiconductor field effect transistor.

[c6] 6.The cross-coupled inverter of claim 2 wherein the first NFET, the second NFET, the first PFET and the second PFET each comprises a triple-well metal-ox-ide-semiconductor field effect transistor.

[c7] 7.The cross-coupled inverter of claim 1 wherein:
the body of the first NFET is coupled to the body of the second NFET; and
the body of the first PFET is coupled to the body of the second PFET.

[c8] 8.The cross-coupled inverter of claim 7 wherein the first NFET, the second NFET, the first PFET and the second PFET each comprises a silicon-on-insulator metal-oxide-semiconductor field effect transistor.

[c9] 9.The cross-coupled inverter of claim 7 wherein the first NFET, the second NFET, the first PFET and the second PFET each comprises a triple-well metal-oxide-semiconductor field effect transistor.

[c10] 10.The cross-coupled inverter of claim 1 further comprising:
a first capacitor that couples the body and the drain of the first NFET;
a second capacitor that couples the body and the drain of the first PFET;
a third capacitor that couples the body and the drain of the second NFET; and
a fourth capacitor that couples the body and the drain of the second PFET.

[c11] 11.The cross-coupled inverter of claim 10 wherein the drain of the first NFET is coupled to the drain of the first PFET.

[c12] 12.The cross-coupled inverter of claim 10 wherein the drain of the second NFET is coupled to the drain of the

second PFET.

[c13] 13.The cross-coupled inverter of claim 10 wherein the first NFET, the second NFET, the first PFET and the second PFET each comprises a silicon-on-insulator metal-oxide-semiconductor field effect transistor.

[c14] 14.The cross-coupled inverter of claim 10 the wherein first NFET, the second NFET, the first PFET and the second PFET each comprises a triple-well metal-oxide-semiconductor field effect transistor.

[c15] 15.A method of forming a cross-coupled inverter comprising:
providing a cross-coupled inverter circuit having:
a first inverter circuit including a first NFET coupled to a first PFET, the first NFET and the first PFET each having a body and a drain; and
a second inverter circuit cross-coupled with the first inverter circuit at a plurality of nodes, the second inverter circuit including a second NFET coupled to a second PFET, the second NFET and the second PFET each having a body and a drain; and
coupling the body of at least one of the first NFET, the second NFET, the first PFET and the second PFET so as to form a feedback path that reduces discharging at one or more of the plurality of nodes in response to a soft error

event at the cross-coupled inverter.

[c16] 16.The method of claim 15 wherein coupling the body of at least one of the first NFET, the second NFET, the first PFET and the second PFET so as to form a feedback path comprises:
coupling the body and the drain of the first NFET together;
coupling the body and the drain of the first PFET together;
coupling the body and the drain of the second NFET together; and
coupling the body and the drain of the second PFET together.

[c17] 17.The method of claim 16 further comprising coupling the body and the drain of the first NFET to the body and the drain of the first PFET.

[c18] 18.The method of claim 16 further comprising coupling the body and the drain of the second NFET to the body and the drain of the second PFET.

[c19] 19.The method of claim 16 wherein coupling the body and the drain of the first NFET together comprises resistively coupling the body and the drain of the first NFET together.

[c20] 20.The method of claim 15 wherein coupling the body of at least one of the first NFET, the second NFET, the first PFET and the second PFET so as to form a feedback path comprises:

coupling the body of the first NFET to the body of the second NFET; and

coupling the body of the first PFET to the body of the second PFET.

[c21] 21.The method of claim 15 wherein coupling the body of at least one of the first NFET, the second NFET, the first PFET and the second PFET so as to form a feedback path comprises:

capacitively coupling the body and the drain of the first NFET;

capacitively coupling the body and the drain of the first PFET;

capacitively coupling the body and the drain of the second NFET; and

capacitively coupling the body and the drain of the second PFET.